REMARKS

We are in receipt of the Office Action dated September 25, 2001, in connection with the above-identified application, and the accompanying Amendment and following remarks are made in light thereof.

Claims 1-26 are pending in the application. All 26 claims stand rejected pursuant to the Office Action.

Initially, claims 1-26 stand rejected under 35 USC 112, second paragraph. In response, these claims have been amended to expressly recite that the second conductive layer partially overlaps the impurity region of each of TFT's, particularly in light of the Examiner's comment in Paragraph 7 of the Office Action.

Claims 11-13 are rejected under 35 USC 103(a) as being unpatentable over Miyaska et al.. In response to this rejection, claim 11 has been amended to delete the term "electrically" in order to clarify that the third impurity region constitutes the source or drain region. Applicant believes that this Amendment overcomes this rejection since Miyaska et al. fail to disclose that the second gate electrode in the p-channel TFT partially overlapping the third impurity region which constitutes the source or drain region.

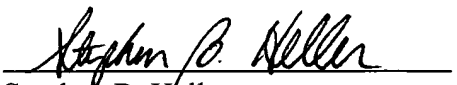
Claims 1-10 are rejected under 35 USC 103(a) as being unpatentable over Miyasaka et al. in view of Kondo. In response, independent claims 1 and 6 have been amended to expressly recite

that the second conductive layer of the p-channel TFT partially overlaps the source and drain regions while the second conductive layer of the n-channel TFT partially overlaps the LDD region. In the claimed invention, the semiconductor layer of the p-channel TFT has no LDD regions because it is preferred to balance characteristics between the n-channel TFT and the p-channel TFT that is inherently high in reliability by gaining ON-current. (Please see the specification page 20, lines 8-14). Referring to Miyaska et al., it appears that the LDD region is provided in the p-channel TFT and the gate electrode does not overlap the source and drain regions. Further, it appears that Kondo does not expressly teach or suggest the p-channel TFT in which the second conductive layer partially overlaps the source and drain regions. Therefore, Applicant believes that this Amendment sufficiently distinguishes the present invention from Miyasaka et al. and Kondo or the combination thereof.

In response to remaining 103(a) rejections of claims 14-26 based on Miyasaka et al. in view of Kondo (claims 14-23), further in view of Johnson (claims 24-26), Applicant has amended independent claims 14, 19 and 24 similarly to claims 1, 6 and 11.

Accordingly, in view of the foregoing, Applicant respectfully requests reconsideration and allowance of the pending claims.

Respectfully submitted,



Stephen B. Heller
Registration No.: 30,181

COOK, ALEX, McFARRON, MANZO
CUMMINGS & MEHLER, LTD.
200 West Adams Street, Suite 2850
Chicago, Illinois 60606
(312)236-8500

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1 (Thrice Amended). A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surface of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and [a third impurity region being in contact with said second channel formation region] second source and drain regions,

wherein [said first impurity region of said n-channel TFT is disposed so as to partially overlaps with a portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein [said third impurity region of said p-channel TFT is disposed so as to partially overlaps with said portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions.

5 (Amended). A ferroelectric liquid crystal display device according to claim 1, wherein said [first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region] semiconductor layer of said p-channel TFT has no LDD regions.

6 (Twice Amended). A ferroelectric liquid crystal display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surface of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and [a third impurity region being in contact with said second channel formation region] second source and drain regions,

wherein [said first impurity region of said n-channel TFT is disposed so as to partially overlaps with a portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein [said second impurity region of said n-channel TFT is disposed so as not to overlaps with said second conductive layer] the portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT does not overlap said second source and drain regions;

wherein [said third impurity region of said p-channel TFT is disposed so as to partially overlaps with said portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlaps said second source and drain regions.

10 (Amended). A ferroelectric liquid crystal display device according to claim 6, wherein said [first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region] semiconductor layer of said p-channel TFT has no LDD regions.

11 (Twice Amended). A ferroelectric liquid crystal display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said [first impurity region is disposed so as to partially overlaps with said first gate electrode] first gate electrode partially overlaps said first impurity region, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein [said third impurity region is disposed so as to partially overlaps with said second gate electrode] second gate electrode partially overlaps said third impurity region, and

wherein a wiring is [electrically] connected to said third impurity region.

12 (Amended). A ferroelectric liquid crystal display device according to claim 11, wherein said first and second gate electrodes comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).

14 (Twice Amended). A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surface of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region, and a second

impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and [a third impurity region being in contact with said second channel formation region] second source and drain regions,

wherein [said first impurity region of said n-channel TFT is disposed so as to partially overlaps with a portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein [said third impurity region of said p-channel TFT is disposed so as to partially overlaps with said portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT is partially overlaps said second source and drain regions.

18 (Amended). A goggle type display device according to claim 14, wherein said [first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region] semiconductor layer of said p-channel TFT has no LDD regions.

19 (Twice Amended). A goggle type display device having a CMOS circuit comprising an n-channel TFT and a p-channel TFT, said CMOS circuit comprising:

each gate electrode of said n-channel TFT and said p-channel TFT having a first conductive layer being in contact with a gate insulating film, and a second conductive layer being in contact with said gate insulating film and top and side surface of said first conductive layer;

a semiconductor layer of said n-channel TFT comprising a first channel formation region, [a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region] a pair of LDD regions and first source and drain regions; and

a semiconductor layer of said p-channel TFT comprising a second channel formation region and [a third impurity region being in contact with said second channel formation region] second source and drain regions,

wherein [said first impurity region of said n-channel TFT is disposed so as to partially overlaps with a portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said n-channel TFT partially overlaps said pair of LDD regions;

wherein [said second impurity region of said n-channel TFT is disposed so as not to overlaps with said second conductive layer] the portion which said second conductive layer is in contact with said gate insulating film in said n-channel region does not overlap said first source and drain regions;

wherein [said third impurity region of said p-channel TFT is disposed so as to partially overlaps with said portion which said second conductive layer is in contact with said gate insulating film] a portion which said second conductive layer is in contact with said gate insulating film in said p-channel TFT partially overlap said second source and drain regions.

23 (Amended). A goggle type display device according to claim 19, wherein said [first impurity region is a LDD region, said second impurity region is a source or a drain region, and said third impurity region is the source or the drain region] semiconductor layer of said p-channel TFT has no LDD regions.

24 (Twice Amended). A goggle type display device having an n-channel TFT and a p-channel TFT over a substrate,

said n-channel TFT comprising:

a first gate electrode formed adjacent to a first semiconductor layer with a first gate insulating film interposed therebetween, said first semiconductor layer comprising a first channel formation region, a first impurity region being in contact with said first channel formation region, and a second impurity region being in contact with said first impurity region;

wherein said [first impurity region is disposed so as to partially overlaps with said first gate electrode] first gate electrode partially overlaps said first impurity region, and

said p-channel TFT comprising:

a second gate electrode formed adjacent to a second semiconductor layer with a second gate insulating film, said second semiconductor layer comprising a second channel formation region and a third impurity region being in contact with said second channel formation region,

wherein said [third impurity region is disposed so as to partially overlaps with said second gate electrode] second gate electrode partially overlaps said third impurity region, and

wherein a wiring is [electrically] connected to said third impurity region.

25 (Amended). A goggle type display device according to claim 24, wherein said first and second gate electrodes comprise a material selected from the group consisting of titanium (Ti), tantalum (Ta), tungsten (W), and molybdenum (Mo).